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VERIFICATION OF A TRANSLATION

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My name and post office address are as stated below;

That I am knowledgeable in the German language in which the below identified international application was filed, and that, to the best of my knowledge and belief, the English translation of the amended sheets of the international application No. PCT/DE03/02352 is a true and complete translation of the above identified international application as filed.

I hereby declare that all the statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the patent application issued thereon.

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1A with a (100) surface orientation, in which case it is preferable to use a Si substrate. To achieve a high-quality starting surface and to bury the interface states at the interface between 1B and 1A, it is possible, in accordance with Figure 3A, by way of example, for a semiconductor buffer layer 1B to be deposited epitaxially, in which case it is preferable for a silicon buffer layer to be deposited by means of a molecular beam epitaxy (MBE) process or a MOCVD (metal organic chemical vapor deposition) process. Particularly when using an MBE process, this treatment step results in a starting surface which has been smoothed to a range of one atom layer. The thickness of the buffer layer 1B is in this case determined only by a processing rate (throughput) and a predetermined starting quality.

As an alternative to the smoothing process described above, it is also possible to carry out conventional smoothing processes, such as for example CMP (chemical mechanical polishing) processes.

Then, a crystalline stress generator layer SG is formed on the carrier material 1 or the smooth starting surface of the semiconductor buffer layer 1B, the crystal structure of this stress generator layer SG substantially having a first lattice constant for the purpose of generating a mechanical stress in the stress-absorbing semiconductor layer which is subsequently formed.

By way of example, the stress generator layer SG includes a IV-IV semiconductor or a III-V semiconductor. However, it may also include a multilayer sequence and/or change gradually by means of

a molecular beam epitaxy process, which in turn results in improved ongrowth properties for the subsequent layers. In particular when an Si layer is used as stress-absorbing semiconductor layer SA, it is preferable for $Si_{1-x}Ge_x$ to be used as semiconductor material for the stress generator layer SG,